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FOR

A METHOD AND SYSTEM FOR A HIGH-DENSITY PLASMA DEPOSITION PROCESS FOR FABRICATING A TOP CLAD FOR PLANAR LIGHTWAVE CIRCUIT DEVICES

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A METHOD AND SYSTEM FOR A HIGH-DENSITY PLASMA DEPOSITION PROCESS FOR FABRICATING A TOP CLAD FOR PLANAR LIGHTWAVE CIRCUIT DEVICES

FIELD OF THE INVENTION

The present invention relates generally to the fabrication of planar lightwave circuits. More particularly, the present invention relates to a method and system for a high-density plasma deposition process for fabricating a top clad for an arrayed waveguide grating planar lightwave circuit.

BACKGROUND OF THE INVENTION

Planar lightwave circuits (PLCs) comprise fundamental building blocks for the modern fiber optic communications infrastructure. Planar lightwave circuits are generally devices configured to transmit light in a manner analogous to the transmission of electrical currents in printed circuit boards and integrated circuit devices. Examples include arrayed waveguide grating devices, integrated wavelength multiplexers/demultiplexers, optical switches, optical modulators, wavelength-independent optical couplers, and the like.

PLCs generally involve the provisioning of a series of embedded optical waveguides upon a semiconductor substrate, with the optical waveguides

fabricated from a silica glass. Planar lightwave circuits are constructed using the advanced tools and technologies developed by the semiconductor industry. Modern semiconductor electronics fabrication technology can aggressively address the increasing need for integration is currently being used to make PLCs. By using manufacturing techniques closely related to those employed for silicon integrated circuits, a variety of optical elements can be placed and interconnected on the surface of a silicon wafer or similar substrate. This technology has only recently emerged and is advancing rapidly with leverage from the more mature tools of the semiconductor-processing industry.

PLCs are constructed with a number of waveguides precisely fabricated and laid out across a silicon wafer. A conventional optical waveguide comprises an undoped silica bottom clad layer, with at least one waveguide core formed thereon, and a cladding layer covering the waveguide core, wherein a certain amount of at least one dopant is added to both the waveguide core and the cladding layer so that the refractive index of the waveguide core is higher than that of the cladding layer. Fabrication of conventional optical waveguides involves the formation of an undoped silica layer as the bottom clad (BC), usually grown by thermal oxidation upon a silicon semiconductor wafer. The core layer is a doped silica layer, which is deposited by either plasma-enhanced chemical vapor deposition (PECVD) or flame hydrolysis deposition (FHD). An annealing procedure then is applied to this core layer (heated above 1000C) not only to expel the undesired chemical substance such as the radicals with bonded hydrogen but also to reduce the inhomogenities of refractive index within the core layer. The waveguide pattern is defined by photolithography on the core layer, and reactive ion etch (RIE) is used to remove the excess doped silica to form waveguide core. A SiO2 cladding layer

is then formed through a subsequent deposition process. Finally, the wafer is cut into multiple planar lightwave circuit dies and packaged according to their particular applications.

Prior art Figure 1 shows a cross-section view of a conventional planar optical waveguide. As depicted in Figure 1, the planar optical waveguide includes three doped SiO_2 glass cores 10a-10c formed over a SiO_2 silica bottom clad 12. A BPSG top cladding layer 11 covers both the cores 10a-c and the bottom clad 12. As described above, the refractive index of the cores 10a-c is higher than that of the top cladding layer 11 and the bottom clad 12. Consequently, optical signals are confined axially within cores 10a-c and propagate lengthwise through cores 10a-c. The cores 10a-c are typically doped with Germanium to increase their index of refraction.

Arrayed waveguide grating planar lightwave circuits are one of the most precisely manufactured PLCs. Arrayed waveguide grating devices are used to implement multiplexing or demultiplexing functions within a fiber-optic network. A typical arrayed waveguide grating device is configured for multiplexing or demultiplexing, for example, 16 channels with a separation of 100 gigahertz between the channels. Arrayed waveguide grating devices having 40 channels spaced at 50 gigahertz are commercially available, and even more advanced devices having 128 channels spaced at 25 gigahertz have been demonstrated. Such advanced arrayed waveguide grating devices have enabled the provisioning of dense wave division multiplexing (DWDM) fiber-optic networks, which are increasingly being relied upon to handle the geometrically expanding demand for data transfer bandwidth.

The performance of such advanced arrayed waveguide grating devices (e.g., 40 channels or more) is critically dependent upon the performance of the semiconductor manufacturing technologies used to fabricate them. For example, a 128 channel arrayed waveguide grating device will have at least 128 precisely defined optical waveguides fabricated therein. Small defects, anomalies, imperfections, or the like, have very significant impacts upon the performance of an arrayed waveguide grating device. Any such defect, for example, can directly affect the channel isolation of any of the waveguides within the affected area of the defect, cause signal loss from waveguides within the affected area, or the like. Hence, to maintain acceptable yields while providing the required performance, it becomes extremely important to ensure the fabrication of the optical waveguides of the arrayed waveguide grating devices are as precise and deterministic as possible.

Prior art Figures 2A through 2C depict a top clad deposition process wherein three waveguide cores 21-23 are covered during a deposition process to form the top clad (e.g., top cladding layer 11). A well known problem with the fabrication of an arrayed waveguide grating devices is the gap fill of high aspect ratio areas between optical waveguide cores during top clad deposition. Figure 2A shows three cores 21-23 out of the numerous waveguide cores comprising, for example, a 16 channel arrayed waveguide grating device. Figure 2B shows three waveguides 21-23 at an intermediate step of the top clad deposition process. As shown in Figure 2B, the gaps between cores 21-23 have been partially filled by the top clad layer 25. Subsequently, as shown in Figure 2C, when the top clad deposition process is complete, the gaps between cores 21-23 are completely filled and the top clad layer 26 is completely flat and without voids.

Prior art Figure 3 shows the problems which occur during a top clad deposition process of a highly integrated PLC device. Figure 3 shows three cores 31-33 which are more closely spaced with respect to waveguides 21-23 of Figure 2. As is well known, the closely spaced cores 33-31 present high aspect ratio gaps between them which must be filled during the top clad deposition process. The high aspect ratio of the gaps causes micro voids 41 and 42 to form as top clad layer 37 is deposited. The voids 41-42 are serious defects which significantly affect the performance of the waveguides comprising cores 31-33. In a case where the defects are not so significant as to create voids, there may be low density areas within the gaps instead of voids. Crystallization will develop in these low density areas. The areas of local crystallization also adversely affects the performance of the waveguides. Typical prior art top clad deposition processes (e.g., PECVD) can only fill gaps larger than 2 microns (e.g., at an aspect ratio of 3) or larger while ensuring the absence of voids or local crystallization problems.

One solution to this problem is to utilize a very gradual top clad "buildup" process, wherein a number of deposition and anneal cycles are used to gradually buildup the thickness of the top clad layer. Successive thin top clad layers (e.g., typically 4 layers at minimum) are deposited and annealed in an attempt to avoid the formation of voids. While this solution is somewhat effective in filling high aspect ratio gaps, the large number of deposition and anneal cycles greatly decreases the throughput of the fabrication line.

Thus what is needed is a solution that can effectively fill high aspect ratio gaps between waveguide cores of an arrayed waveguide grating PLC

device. What is needed is a solution that can fill high aspect ratio gaps without adding an excessive amount of time to the overall device fabrication process. What is further required is a solution that can fill high aspect ratio gaps while ensuring no voids or crystallization problems occur. The present invention provides a novel solution to the above requirements.

SUMMARY OF THE INVENTION

The present invention is a high-density plasma deposition process for fabricating a top clad that can effectively fill high aspect ratio gaps between waveguide cores of an arrayed waveguide grating planar lightwave circuit device. The present invention provides a solution that can fill high aspect ratio gaps while reducing the overall device fabrication process time. Additionally, the present invention provides a solution that can fill high aspect ratio gaps while ensuring no voids or crystallization problems occur.

In one embodiment, the present invention is implemented as a high-density plasma (HDP) deposition process for fabricating a top clad for an arrayed waveguide grating PLC. The HDP deposition process is optimized for performing high aspect ratio gap fill during PLC top clad deposition. During fabrication of the arrayed waveguide grating device, a plurality of waveguide cores are formed on a bottom clad, the waveguide cores having a plurality of gaps there between. The refractive index of the waveguide cores are controlled by using a dopant to be higher than the refractive index of the cladding layer. A cladding layer is formed over the waveguide cores and the bottom clad using an HDP deposition process. The HDP deposition process effectively fills the gaps between the cores. The gaps between the waveguide cores can be smaller than 2 microns. The aspect ratio of the gaps between the waveguide cores can be greater than 3. A one step HDP deposition process can fill the gaps completely. An anneal process is performed on the cladding layer after the HDP deposition process. The HDP deposition process provides a very high purity USG (undoped silica glass) layer having a uniform refractive index. Subsequently, an overlying layer of doped silica glass (e.g., BPSG) can be

deposited over the cladding layer using a conventional plasma enhanced chemical vapor deposition (PECVD) process in a one step deposition and anneal cycle to obtain the desired thickness.

The process of the present invention enhances device yield due to the fact that the HDP deposition process can fill high aspect ratio gaps while greatly reducing the number of deposition and anneal cycles, and thus time, of the overall device fabrication process. Additionally, the HDP deposition process solves crystallization problems in the gap areas experienced in the prior art.

In another embodiment, the HDP deposition process is used to deposit a BPSG top clad instead of a USG top clad to reduce the top clad stress. Boron and phosphene is added during the HDP deposition to adjust the CTE (coefficient of thermal expansion) of the top clad (e.g., the resulting CTE of the top clad after anneal) to match the CTE of the silicon substrate. This greatly reduces PDW effects within the PLC device.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not by way of limitation, in the Figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Prior art Figure 1 shows a cross-section view of a conventional planar optical waveguide fabricated using a silica glass substrate.

Prior art Figure 2A shows three cores of three optical waveguides of a typical arrayed waveguide grating device.

Prior art Figure 2B shows three waveguide cores of three waveguides of a typical arrayed waveguide grating device at an intermediate step of a top clad deposition process.

Prior art Figure 2C shows three waveguide cores of three waveguides of a typical arrayed waveguide grating device at the completion of the top clad deposition process.

Figure 3 shows a cross-section view of an optical waveguide structure fabricated in accordance with a waveguide core layer over-etch process of the present invention.

Figure 4 shows a cross-section view of an optical waveguide structure prior to an HDP deposition process of the present invention.

Figure 5 shows a cross-section view of an optical waveguide structure after the HDP deposition process of the present invention has commenced.

Figure 6 shows a cross-section view of the optical waveguide structure after the HDP deposition process is complete.

Figure 7 shows a cross-section view of the optical waveguide structure after a PECVD deposition of an overlying BPSG layer.

Figure 8 shows a cross-section view of the optical waveguide structure with an HDP deposited BPSG layer and an overlying PECVD BPSG layer as the top clad.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to obscure aspects of the present invention unnecessarily.

Embodiments of the present invention are directed towards an HDP deposition process for fabricating a top clad that can effectively fill high aspect ratio gaps between waveguide cores of an AWG and other types of PLC devices. The present invention provides a solution that can fill high aspect ratio gaps while reducing the overall device fabrication process time. Additionally, the present invention provides a solution that can fill high aspect ratio gaps while ensuring no voids or crystallization problems occur. The present invention and its benefits are further described below.

Figure 4 shows a cross-section view 400 of an optical waveguide structure fabricated in accordance with an HDP deposition process of the present invention. As depicted in Figure 4, optical waveguide structure 400 is shown in a state subsequent to etching to remove a core layer used to form core 401 and core 402. Cores 401-402 are disposed on a bottom clad layer 403.

As depicted in Figure 4, cores 401-402 are disposed very close together on bottom clad 403, thereby forming a high aspect ratio gap 410 between them. It is critical that the high aspect ratio gap 410 be effectively filled during subsequent top clad deposition. As used herein, the term aspect ratio refers to the height of the cores 401-402 divided by the width of the gap 410 between them. For example, in a case where the cores 401-402 are 6 microns high (e.g., from the top of the cores to bottom clad) and the gap 410 is 1 micron wide, the aspect ratio is 6. AWG devices and other related PLC devices are highly dependent upon the precise fabrication of closely spaced optical waveguides such as cores 401-402. The present invention ensures effective gap fill by using an HDP deposition process to lay down a top clad.

Figure 5 shows a cross-section view 500 of the optical waveguide structure after an HDP deposition process in accordance with the present invention. As depicted in Figure 5, a HDP layer 501 has been deposited across cores 401-402 and bottom clad 403. The HDP deposition process is optimized for performing high aspect ratio gap fill during planar lightwave circuit top clad deposition. The HDP deposition process effectively fills the gap 410 between the cores 401-402. The gap 410 can be smaller than 2 microns, and have an aspect ratio greater than 3. In this embodiment, HDP layer 501 is a USG (undoped silica glass) layer.

HDP deposition is an emerging technology based on the use of high-density plasma to ensure gap fill. High-density plasma is used to impart simultaneous chemical vapor deposition (e.g., SiO_2) and the sputter etching of the target (e.g., the deposited layer) from bombarding ions. Void free gap filling occurs within narrow spaces with high aspect ratios by depositing SiO_2 under continuous ion bombardment. The ion bombardment removes material building up at the upper corners of the gaps. The removal of this material greatly reduces the likelihood of void formation.

Figure 6 shows a cross-section view 600 of the optical waveguide structure after the HDP deposition process is complete. Cross-section view 600 shows the top clad layer 501 after completion of the HDP deposition process, showing the completed top clad layer 501 at the same height as cores 401-402 (e.g., 6 microns). The cores 401-402 have residual HDP layer peaks 601-602 disposed above them. Thus, using the HDP deposition process of the present invention, the top clad layer 501 can be completed in a single deposition cycle, and subsequent annealing. In contrast, prior art top clad deposition processes (e.g., PECVD) cannot fill gaps any smaller than 2 microns (e.g., having an aspect ratio of 3) without experiencing significant void and crystallization problems. Since an HDP deposition process applies deposition and etch at same time, the material inside gap 410 is much more dense than possible with, for example, a PECVD deposition process. The higher density provides for a much more effective fill of high aspect ratio (e.g., aspect ratio 9) gaps without any micro void formation or crystallization problems.

Figure 7 shows a cross-section view 700 of the optical waveguide structure after a PECVD deposition of an overlying PECVD layer 701. In this embodiment, HDP deposition is used to fill the gap between the cores 401-402 (e.g., 6 microns deep) in a single deposition step. Then, a thick layer of BPSG (e.g., 10 to 14 microns deep) is deposited using conventional PECVD. The PECVD layer 701 can be deposited on the top of HDP deposition formed layer 501 without difficulty. In this embodiment, PECVD is used to form layer 701 since the PECVD deposition rate is faster than the HDP deposition rate. Once the gaps are filled, the faster PECVD processing can be taken advantage of.

It should be noted that production cycle time is greatly reduced in comparison to the prior art, due to the fact that 6 or 7 deposition/anneal steps are required in a prior art PECVD BPSG (Boron Phosphorous silica glass) top clad deposition process and 4 deposition/anneal steps are required in prior art PECVD BPSG top clad deposition process. In contrast, the USG HDP deposition process of the present invention is accomplished in a single step.

It should also be noted that GeBPSG (Germanium Boron Phosphorous silica glass) can also be deposited as the PECVD layer 701 instead of PBSG.

Figure 8 shows a cross-section view 800 of an optical waveguide structure in accordance with an alternative embodiment of the present invention. In this embodiment, the HDP deposition process is used to deposit a BPSG HDP layer instead of a USG HDP layer. BPSG is deposited to reduce the top clad stress. Boron and phosphene is added during the HDP deposition of HDP layer 801 to adjust the CTE (coefficient of thermal expansion) of the top clad (e.g., the resulting CTE of the top clad after anneal) to match the CTE

of the silicon substrate. This greatly reduces PDW effects within the PLC device. PECVD is used to form PECVD layer 701, in the same manner described above.

Thus, embodiments of the present invention are directed towards an HDP deposition process for fabricating a top clad that can effectively fill high aspect ratio gaps between waveguide cores of an AWG PLC device. The present invention provides a solution that can fill high aspect ratio gaps while decreasing the overall device fabrication process time. Additionally, the present invention provides a solution that can fill high aspect ratio gaps while ensuring no voids or crystallization problems occur.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order best to explain the principles of the invention and its practical application, thereby to enable others skilled in the art best to utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.